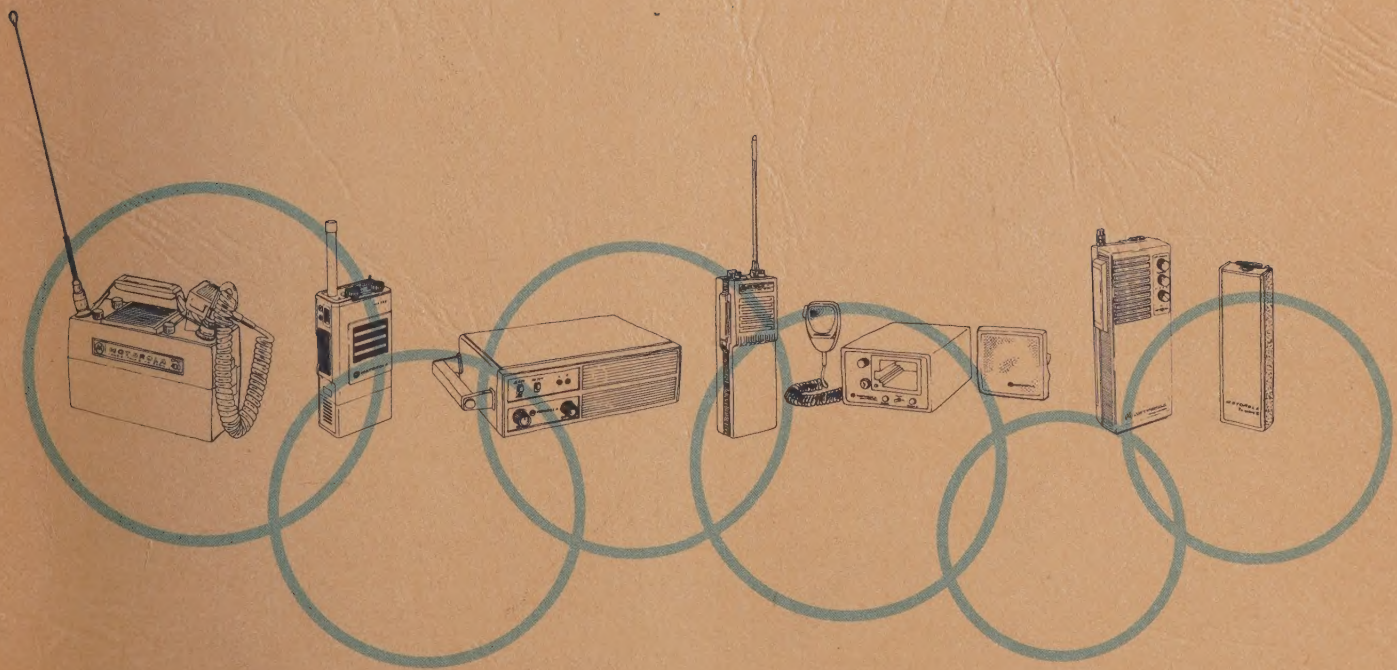
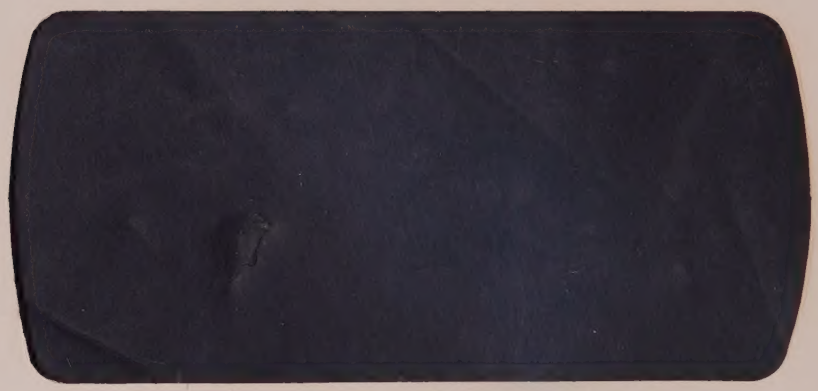
MOTOROLA

SP4900841

METRO-PAGEBOY" BINARY ENCODER



Communications Products Division
8000 W. SUNRISE BLVD. FT. LAUDERDALE, FL 33322



SP4900841

"METRO-PAGEBOY" BINARY ENCODER

MOTOROLA INC. Communications Division

ENGINEERING PUBLICATIONS 8000 W. SUNRISE BLVD., FT. LAUDERDALE, FL 33313

Copyright 1974 by Motorola, Inc.
Printed in U.S.A.

3/8/76

1S-SP490084
Issue-2

TABLE OF CONTENTS

1. DESCRIPTION 3

2. MODEL COMPLEMENT 3

3. INSTALLATION 3

4. OPERATION

   a. Operating Controls and Indicators 4
   b. Operation as a Test Encoder 6
   c. Operation as a Manual Paging Encoder 7
   d. Wiring Options 8

5. THEORY OF OPERATION

   a. Code Entry Lever Switches 8
   b. BCD-to-Binary Converter 8
   c. Switchable Inverter 9
   d. ROM (Word 1 Table) 9
   e. W1/W2 Select 14
   f. Shift Register/Parity Generator 14
   g. Output Multiplexer 14
   h. Clock Oscillator 14
   i. Timing and Control Logic 15
   j. Output Amplifier 18
   k. Power Supply 19

6. PARTS LISTS 20

7. ATTACHMENTS 25

1. DESCRIPTION

The "Metro-Pageboy" Binary Encoder is a special paging encoding device designed for use in maintaining "Metro-Pageboy" binary paging receivers. It may also be used as a manually-operated encoder for small demonstration systems. The unit accepts as input any six-digit decimal number in the range 000002 through 399999, giving a code capability of almost 400,000 separate codes. However, certain codes in this range are considered by the encoder as being illegal and are indicated as such by the illumination of an "illegal code" indicator on the front panel of the unit. The illegal codes can be represented by 00XY00 and 00XY01 where X and Y can be any decimal digit.

The encoder provides for a symmetrical output signal which is adjustable from 0 to ±6 volts. It is intended to be used in conjunction with a signal generator having a dc-coupled direct FM input capability, such as the Motorola S1300 Series Signal Generators. Nominal input power applied to the unit can be either 117 V or 234 V, 50 or 60 Hz, selected by internal wiring options.

2. MODEL COMPLEMENT

The following special circuit boards and assemblies are included in the "Metro-Pageboy" binary encoder.

- SP49008411 Main Chassis
- SP49008412 Power Supply Board
- SP49008413 Main Logic Board
- SP49008414 Leverwheel Board

3. INSTALLATION

The "Metro-Pageboy" binary encoder is a completely self-contained unit and no special installation requirements are necessary. An eight-foot power cord and plug is provided for connecting the unit to the primary ac power source. The encoder is normally shipped for use with 117 V, 50 or 60 Hz power sources. If it is desired to use the unit with a nominal 234 V, 50 or 60 Hz source, it is only necessary to change two wires on the input power transformer. Refer to Figure 2 to implement these wiring changes.

4. OPERATION

a. Operating Controls and Indicators

All controls and indicators are located on the front panel of the unit, while terminals for external connections are mounted at the rear. Table 1 lists all panel designations, types, and functional uses of each control, indicator, and terminal on the encoder.

Table 1. Controls and Indicators

Panel Designation	Type	Use
CODE	6-section lever-wheel switch	Sets desired code number into unit.
OFF/SINGLE/CONT	3-position rotary switch and light-emitting diode	Applies power to unit and selec either single (SINGLE) or cont uous (CONT) mode of operatio
SEND	Pushbutton switch and light-emitting diode	Starts paging sequence in accordance with the setting of OFF/SINGLE/CONT switch.
INVERT/NON-INVERT	Toggle switch	Selects polarity of output signa
OUTPUT LEVEL	Potentiometer	Controls output voltage level.
OUTPUT	Binding posts	Provides output connection for u
ILLEGAL CODE	Light-emitting diode	Indicates that an illegal code h been entered into the encoder.
(See below)	8-terminal barrier strip	Provides for external connecti to unit.

The numbers inserted into the encoder by the CODE switches should agree with the code marked on the pager code plug. If the pager is a dual-function pager, the code plug is marked with a six-digit number followed by a slash (/) which, in turn, is followed by a two-digit number. To activate the first function, set the CODE switches to the first six-digit number; to activate the second function, set the switches to the first four digits of the six-digit number and then to the two digits following the slash. For exampl if the number on the code plug is 101022/23, the first function code number is 101022 and the second is 101023.

Power is applied to the unit when the OFF/SINGLE/CONT switch is placed in either the SINGLE or CONT position at which time the light-emitting diode indicator should light. This switch operates in conjunction with the SEND pushbutton in the following manner. When the pushbutton

is depressed and released, and the mode switch is in the SINGLE position, a single page sequence is initiated. This consists of a 1.25-second preamble, word 1 of the pager address, a half-bit space, and word 2 of the pager address, after which the encoder returns to the non-sending mode. With the mode switch in the CONTinuous position, depressing and releasing the SEND pushbutton starts a continuous paging sequence consisting of a 1.25-second preamble, word 1 of the pager address, a half-bit space, word 2 of the pager address, a 14-bit "comma", word 1, half-bit space, word 2, "comma", etc. until the SEND switch is depressed and released a second time, or the mode switch is placed in the SINGLE position.

The INVERT/NON-INVERT switch determines the logical significance of the output signal. In the NON-INVERT position, a positive voltage output signal corresponds to a binary 1 and a negative voltage output corresponds to a binary 0. In the INVERT position, these relationships are reversed. When using the encoder with a signal generator in which a positive modulation voltage results in an increase in frequency, use the NON-INVERT position. When using the encoder with a signal generator in which a positive modulation voltage results in a decrease in frequency, use the INVERT position of the switch.

NOTE

The preceding statements for inversion of the output signal hold only for pagers in which the second conversion oscillator frequency is 17.865 MHz (most carrier frequencies). For pagers in which the second conversion oscillator frequency is 17.935 MHz, the reverse is true.

The eight-position terminal board mounted on the rear of the unit provides for the following external connections:

- W1 SYNC - a pulse coincident with the first bit of word 1 of the pager address.
- W2 SYNC - a pulse coincident with the first bit of word 2 of the pager address.
- T T O - this is a transistor collector which is turned on (to ground) when a page sequence is being sent. It is capable of switching a load of 100 mA, with an open-circuit voltage of up to 30 V dc.
- REMOTE SEND - these are three terminals (N.O., C, and N.C.) which provide for the connection of a remote SPDT switch. Its purpose is to duplicate the functions performed by the SEND pushbutton on the front panel. If no such switch is connected to these terminals, the N.C. and C terminals must be connected together. If the remote switch is used, its common contact must be connected to

- REMOTE SEND (cont'd) - the C terminal, its normally-closed contact to N.C., and its normally-open contact to N.O. With the remote switch connected, actuating and releasing either the SEND switch on the encoder or the remote switch will initiate (or stop) a paging sequence.

The output terminal at the rear is connected to the red OUTPUT binding post on the front panel which is the high side of the encoder output voltage. The GROUND terminal at the rear is common to the OUTPUT, T T O, W1 SYNC, and W2 SYNC terminals.

b. Operation as a Test Encoder

To check the operation of binary receivers, the following procedure for operating the encoder should be used:

(1) Connect the OUTPUT binding post terminals to the modulation inputs of the signal generator; use any dc-coupled FM generator, such as the Motorola S1300 Series.

(2) Set the INVERT/NON-INVERT toggle switch as required for this test (refer to part a. above for explanation of this switch).

(3) Set the mode switch to the SINGLE position.

(4) Adjust the OUTPUT LEVEL control to produce a ±4 kHz frequency deviation of the signal generator waveform.

(5) Using a frequency counter, set the signal generator to the proper carrier frequency, as determined by the particular model of "Metro-Pageboy" pagers being checked.

(6) Set the pager address code (as marked on the pager code plug) on the CODE leverwheel switches.

(7) To make a sensitivity check of the pager, connect the signal generator output to the NEN6080A Radiation Test Fixture and place the pager under test in the fixture; set the signal generator output to the desired test level.

NOTE

Interconnection diagrams of the various test equipment used in this procedure can be found in the instruction manual for the "Metro-Pageboy" Binary Pager (see Motorola Publication 68P81005C05).

(8) Depress and release the SEND pushbutton on the encoder -- pager should alert.

(9) Reset pager and repeat step (8) two more times. If pager alerts three times in three successive tries, reduce the generator output level and repeat the above test. The lowest generator output level at which the pager alerts three times in three tries determines the sensitivity of that pager.

(10) If the pager under test is a dual-function type, repeat step (8) with the second pager address set on the CODE leverwheel switches.

(11) To troubleshoot the decoder portion of binary pagers, set the mode switch on the encoder to the CONT position and connect either the W1 SYNC or W2 SYNC output to the triggering inputs of an oscilloscope. Both "sync" outputs have negative-going edges at the start of their respective words which will enable various parts of the received data to be examined.

c. Operation as a Manual Paging Encoder

To operate the equipment as either a local or remote binary paging encoder, the following procedure should be used:

(1) Connect the OUTPUT binding post terminals to the modulation inputs of the signal generator; use any dc-coupled FM generator such as the Motorola S1300 Series.

NOTE

If a transmitter or other signal source requiring non-symmetrical modulation inputs signals is being used, some sort of interface or level-shifting circuit will be needed between the encoder and the transmitter. If the OUTPUT LEVEL control on the encoder is set to its maximum position, the output of the encoder is compatible with interfaces meeting EIA RS-232 specifications.

(2) If remote actuation of the encoder is desired, either manual or automatic, connect a remote actuator or timer to the REMOTE SEND terminals on the rear of the encoder as described in preceding paragraph a. Binary logic signals ("true" and "not true") compatible with standard transistor-transistor logic (TTL) circuits may be connected directly to the normally-open (N.O.) and normally-closed (N.C.) terminals, respectively, with the common (C) terminal serving as the circuit ground.

(3) If it is desired to key the transmitter either by the SEND pushbutton switch on the encoder or by a remote actuator, the T T O terminal on the rear of the encoder may be used. If the keyed voltage and current are

compatible with the transistor load capabilities of 100 mA at an open-circuit voltage of up to 30 V dc, connect the keying terminal directly to the T T O terminal; otherwise, a relay can be used.

(4) Place the mode switch in the SINGLE position.

(5) Set the desired pager address on the CODE switches.

(6) Page sequences may now be initiated by either the SEND switch on the encoder or by the remote actuator.

d. Wiring Options

Two jumpers (JU1 and JU2) are provided on the main logic board for selecting the output "comma" rate when not sending page data; see Figure 8 for location of these jumpers. The standard connection has jumper JU2 in place, which results in sending the normal "comma" rate of 300 Hz when not sending a page. By removing jumper JU2 and connecting jumper JU1, the output "comma" rate of the encoder will be doubled to 600 Hz. To "Metro-Pageboy" binary pagers, this high frequency for the "comma" will appear as noise and thereby force the pager into the "battery saver" mode of operation; i.e., the pager will be forced into the "battery saver" mode when no page data is being sent by the encoder without the necessity of removing the carrier signal.

5. THEORY OF OPERATION

a. Code Entry Lever Switches

These switches (Figure 3) are binary-coded-decimal (BCD) switches; that is, each switch has four outputs and one common connection with the switching action as shown in Table 2.

The switches correspond to code digits A, B, C, D, E, and F, with A the switch on the left of the front panel, and F on the right. Switches A, B, E, and F are connected to the BCD-to-binary converter and switches C and D are connected to the read-only-memory (ROM) (word 1 table).

b. BCD-To-Binary Converter

This circuitry consists of IC packages U301 through U309, U312, and U313; refer to Figure 5. Circuits U301 through U309 accept as their inputs the output lines from switches A, B, and E, and the 8, 4, and 2 lines of switch F. This circuit converts the BCD data from the switches into an 11-bit binary number. Circuits U312 and U313 form an 11-input NOR gate

whose output is a high level whenever switches A, B, and E are set to 0, and switch F is set to either 0 or 1. These codes are illegal, and whenever such a code is received, the output of the NOR gate goes high, which in turn causes the output of U313A to go low, illuminating the ILLEGAL CODE indicator.

Table 2. Code Entry Switch Truth Table

SWITCH POSITION	OUTPUT LINE			
	8	4	2	1
0	O	O	O	O
1	O	O	O	C
2	O	O	C	O
3	O	O	C	C
4	O	C	O	O
5	O	C	O	C
6	O	C	C	O
7	O	C	C	C
8	C	O	O	O
9	C	O	O	C

NOTE: C = Connected to common (+5 volts)
O = Open Circuit

c. Switchable Inverter

This inverter circuit consists of exclusive-OR gates U314, U315, and U316. There are two sets of inputs to this circuit. One is the 1 output of switch F, buffered by U310E and U327D. The other set is the 11-bit output of the BCD-to-binary converter. The outputs of this circuit are 12 lines (called word 2, bits 1 through 12). Bit 12 is the same as the 1 output of switch F; bits 1 through 11 are the same as the 11-bit output of the BCD-to-binary converter when bit 12 is low, or 0, and are inverted (i.e.; all low or 0 inputs produce high or 1 outputs, and 1 inputs produce 0 outputs) whenever bit 12 is high, or 1.

d. ROM (Word 1 Table)

The ROM consists of U311. Inputs are the eight outputs of switches C and D, and outputs are 12 lines corresponding to word 1, bits 1 through 12. The complete truth table for this circuit is shown in Table 3.

Table 3. ROM Truth Table (Word 1 Table)

SWITCH SETTINGS			ROM BINARY OUTPUT (12) (1)
CD (DECIMAL)	C OUTPUT (BCD)	D OUTPUT (BCD)	
00	0000	0000	001 011 010 001
01	0000	0001	110 100 101 110
02	0000	0010	101 010 101 011
03	0000	0011	010 101 010 100
04	0000	0100	101 110 001 000
05	0000	0101	010 001 110 111
06	0000	0110	010 101 101 011
07	0000	0111	101 010 010 100
08	0000	1000	011 000 101 010
09	0000	1001	100 111 010 101
10	0001	0000	011 010 101 100
11	0001	0001	100 101 010 011
12	0001	0010	101 001 011 010
13	0001	0011	010 110 100 101
14	0001	0100	011 011 010 011
15	0001	0101	100 100 101 100
16	0001	0110	101 000 010 100
17	0001	0111	010 111 101 011
18	0001	1000	010 101 100 000
19	0001	1001	101 010 011 111
20	0010	0000	101 010 000 100
21	0010	0001	010 101 111 011
22	0010	0010	001 010 111 000
23	0010	0011	110 101 000 111
24	0010	0100	011 010 000 011

Table 3. ROM Truth Table (Word 1 Table) (cont'd)

SWITCH SETTINGS			ROM BINARY OUTPUT (12) (1)
CD (DECIMAL)	C OUTPUT (BCD)	D OUTPUT (BCD)	
25	0010	0101	100 101 111 100
26	0010	0110	111 011 011 000
27	0010	0111	000 100 100 111
28	0010	1000	110 111 100 000
29	0010	1001	001 000 011 111
30	0011	0000	110 101 100 000
31	0011	0001	001 010 011 111
32	0011	0010	010 101 101 000
33	0011	0011	101 010 010 111
34	0011	0100	111 000 001 011
35	0011	0101	000 111 110 100
36	0011	0110	001 101 101 100
37	0011	0111	110 010 010 011
38	0011	1000	110 000 110 100
39	0011	1001	001 111 001 011
40	0100	0000	100 011 101 101
41	0100	0001	011 100 010 010
42	0100	0010	101 000 110 000
43	0100	0011	010 111 001 111
44	0100	0100	001 110 000 011
45	0100	0101	110 001 111 100
46	0100	0110	111 001 100 100
47	0100	0111	000 110 011 011
48	0100	1000	110 000 111 001
49	0100	1001	001 111 000 110

Table 3. ROM Truth Table (Word 1 Table) (cont'd)

SWITCH SETTINGS			ROM
CD (DECIMAL)	C OUTPUT (BCD)	D OUTPUT (BCD)	BINARY OUTPUT (12) (1)
50	0101	0000	100 001 001 100
51	0101	0001	011 110 110 011
52	0101	0010	010 100 000 111
53	0101	0011	101 011 111 000
54	0101	0100	101 000 111 000
55	0101	0101	010 111 000 111
56	0101	0110	011 001 101 111
57	0101	0111	100 110 010 000
58	0101	1000	110 010 010 000
59	0101	1001	001 101 101 111
60	0110	0000	000 101 110 111
61	0110	0001	111 010 001 000
62	0110	0010	010 011 010 000
63	0110	0011	101 100 101 111
64	0110	0100	101 100 001 000
65	0110	0101	010 011 110 111
66	0110	0110	011 100 110 000
67	0110	0111	100 011 001 111
68	0110	1000	000 110 011 000
69	0110	1001	111 001 100 111
70	0111	0000	110 000 110 111
71	0111	0001	001 111 001 000
72	0111	0010	110 100 111 011
73	0111	0011	001 011 000 100
74	0111	0100	001 101 110 010

Table 3. ROM Truth Table (Word 1 Table) (cont'd)

SWITCH SETTINGS			ROM
CD (DECIMAL)	C OUTPUT (BCD)	D OUTPUT (BCD)	BINARY OUTPUT (12) (1)
75	0111	0101	110 010 001 101
76	0111	0110	110 110 001 100
77	0111	0111	001 001 110 011
78	0111	1000	110 011 000 011
79	0111	1001	001 100 111 100
80	1000	0000	011 000 100 111
81	1000	0001	100 111 011 000
82	1000	0010	110 110 000 111
83	1000	0011	001 001 111 000
84	1000	0100	110 001 010 000
85	1000	0101	001 110 101 111
86	1000	0110	101 000 001 100
87	1000	0111	010 111 110 011
88	1000	1000	010 011 100 100
89	1000	1001	101 100 011 011
90	1001	0000	101 000 100 000
91	1001	0001	010 111 011 111
92	1001	0010	011 000 010 000
93	1001	0011	100 111 101 111
94	1001	0100	001 101 000 011
95	1001	0101	110 010 111 100
96	1001	0110	010 110 100 000
97	1001	0111	101 001 011 111
98	1001	1000	000 010 100 000
99	1001	1001	111 101 011 111

e. W1/W2 Select

This consists of U330, U331, and U332. There are two sets of data inputs: the 12 bits of word 1 from the ROM, and the 12 bits of word 2 from the switchable inverter. There is also one control input called the word-select line. The outputs of this circuit are 12 in number, corresponding to bits 1 through 12. When the word-select line is low (logic 0), the outputs correspond to the 12 bits of word 2. When the word-select line is high (logic 1), the outputs correspond to the 12 bits of word 1.

f. Shift Register/Parity Generator

This combination circuit is composed of U333, U334, and U335, which form a 12-stage shift register and U336, which is a parity generator. It has 12 inputs (which are connected to the 12-bit outputs of the W1/W2 select circuit), one output, and three control lines. These three control lines are SRCK1, which is the clock for the shift function; SRCK2, which is the clock for the load function; and LOAD CTL, which controls the shift and load functions. When signal LOAD CTL is high (logic 1), the parallel load function is enabled, and shifting is inhibited; when it is low (logic 0), the shift function is enabled, and loading is inhibited. Both shifting and loading occur on the falling edge of their respective clock inputs. The parity generator is connected to the first, second, third, fourth, fifth, eighth, and eleventh stages of the shift register. Its output, which is connected to the serial input of the 12th stage, is the modulo-2 sum of its inputs. The function of this block is to take the 12-bit parallel input from the W1/W2 select circuit and generate the 23-bit (12 information bits and 11 parity bits) serial form of words 1 and 2.

g. Output Multiplexer

The output multiplexer consists of U310D and F, U336B, and U337. Its function is to select one of four inputs for connection to the output amplifier. The four inputs are the output of the shift register/parity generator, the complement of word 2, bit 1 (generated by U310F), which forms the polarity of the half-bit space between words 1 and 2, the "non-sending" output (which may be at the "comma" rate or at twice that rate, as selected by JU1 or JU2), and the "comma", whose polarity is selected by word 1, bit 1 in U336B. Circuit U310D generates the complement of the output of the multiplexer. The front-panel INVERT/NON-INVERT switch selects either the output of the multiplexer or its complement for connection to the output amplifier.

h. Clock Oscillator

The clock oscillator is a 19.2 kHz crystal oscillator consisting of Y301, Q301, and Q302, with the output buffered by U318A. This oscillator controls all the timing of the encoder.

i. Timing and Control Logic

This circuitry generates all of the timing and control signals for the encoder. Timing diagrams showing the signals generated in the continuous mode and in the single-page mode are shown in Figures 6 and 7, respectively. The functions of the various signals are outlined below.

(1) MPX A and MPX B

These are the control lines to the output multiplexer. The relationship between these signals and the signals selected by the multiplexer is as follows:

MPXA	MPX B	Output Selected
LOW (0)	LOW (0)	1/2-Bit Space Polarity
LOW (0)	HIGH (1)	Shift Register/Parity Generator
HIGH (1)	LOW (0)	Not-Sending Output
HIGH (1)	HIGH (1)	Comma

In addition, MPX A is used as the word-select input to the W1/W2 select circuit and is brought out to the rear panel as W1 SYNC, since the falling edge of this signal occurs at the beginning of the transmission of word 1.

(2) SEND

This signal is the output of flip-flop U317B. It is low (0) when the encoder is not sending, and goes high (1) when the SEND pushbutton is depressed and released. In the continuous mode, it remains high (1) until the SEND pushbutton is again depressed and released; in the single-page mode, it goes low at the end of the first page sequence, when $\overline{\text{COM}}$ goes low.

(3) $\overline{\text{PRE}}$

This signal is the output of counter U328. It is low (0) when the encoder is not sending, or while the preamble is being sent. It goes high (1) at the end of the preamble, and remains high until the SEND signal goes low.

(4) $\overline{\text{COM}}$

This signal is the output of flip-flop U326A. It goes low (0) at the end of the transmission of WORD 2, and remains low while the "COMMA" is being sent. It goes high either at the conclusion of the "COMMA" (continuous mode) or when the SEND signal goes low (single mode).

(5) 1/2 Bit

This signal is the output of U326B. It goes high (logic 1) at the end of word 1, remains high for the duration of the 1/2-bit space, and goes low at the beginning of word 2.

(6) SRCK 1

This signal is the shift clock for the shift register/parity generator. It is low except during transmission of word 1 and word 2; then it is a 300 Hz square wave lasting for 22 cycles for each word.

(7) SRCK 2

This signal is the load clock for the shift register/parity generator. It is a 1200 Hz square wave when the SEND signal is low, and a pulsetrain of 25% duty cycle and 600 Hz repetition rate, as shown in the timing diagrams, when the SEND signal is high.

(8) LOAD CTL

This signal, generated by U337, is the mode control for the shift register/parity generator. When it is high (logic 1), data is parallel-loaded into the shift register under the control of SRCK1, when it is low (logic 0), data is serially shifted under the control of SRCK1. It is high during transmission of the preamble, the comma, and the 1/2-bit space, and low at all other times.

(9) $\overline{\text{W2}}$ SYNC

This signal is the output of flip-flop U326B. It goes low at the beginning of the 1/2-bit space, and high at the end of word 2. It is brought out to the rear panel for oscilloscope synchronization.

(10) Timing and Control Logic

This is made up of several subsections. The output of the clock oscillator is connected to a divider chain consisting of divide-by 16 counter U319 and flip-flops U329A and B. These provide square-wave signals at frequencies of 2400 Hz, 1200 Hz, 600 Hz, and 300 Hz. The 1200 Hz output is connected through gate U320A, to counters U321 and U322. These counters, together with associated gates and flip-flops, control the page sequence timing. In addition, they are used together with counter U32 (and associated gates and flip-flops) to control the preamble timing. Transistor Q303 is connected to the SEND output of U317B, so that when the encoder is sending (SEND is high), Q303 is turned on, thereby turning on

the SEND indicator on the front panel. Transistors Q304 and Q305 form a noninverting switch, connected to the $\overline{\text{SEND}}$ output of U317B, so that when the encoder is sending, Q305 is turned on, shorting the T T O terminal on the rear panel to ground.

When the encoder is not sending, the SEND line is low, and the $\overline{\text{SEND}}$ line is high. The SEND line is connected to NAND gates U320A and U320D, and AND gate U323C. Since the SEND line is low, the outputs of U320A and U320D are high, and the output of U323C is low. The output of U320A is connected to the clock inputs of U321 and U317A; therefore, these clocks are inhibited. The $\overline{\text{SEND}}$ line is connected to the reset line of U328; since this line is high, U328 is reset, causing the $\overline{\text{PRE}}$ line to be low.

Circuits U339A and B form a contact-debouncing circuit for the SEND switch. When the SEND switch is depressed, the output of U339B goes high; when it is released, the output of U339A goes high, causing the output of U339B to go low. Since the output of U339B is connected to the clock input of U317B, the falling edge of the output of U339B causes U317B to toggle, making the SEND output high. This enables the clock inputs of U321 and U317A, which are connected to the 1200 Hz output of U319 through U320A. Circuits U321 and U322 thus begin counting.

Circuits U324A and B, and U323B and C form a gate whose output goes high when the count in U321 and U322 reaches 186, since this line is connected to the input of flip-flop U326A, the output of U326A goes high on the 186th count causing the COM line to go high, and the $\overline{\text{COM}}$ line to go low. Since the $\overline{\text{COM}}$ line is connected to the clock input of U328 through U318D, and both inputs to U318D ($\overline{\text{COM}}$ and $\overline{\text{PRE}}$) are low, the clock input of U328 is high. U323A and U323B form a gate whose output goes high when the count in U321 and U322 reaches 242, since this line is connected to the J input of flip-flop U317A, which is clocked by the gated 1200 Hz output of U319, the output of U317A goes high. This output, together with the 2400 Hz clock, is connected to NAND gate U320C, whose output goes to the $\overline{\text{Reset}}$ input of U317A. Thus, U317A is reset one-half cycle (at 2400 Hz) after it is set. The not-true output of U317A is therefore a negative pulse following the 242 count of U321 and U322.

This pulse (called the COUNT RESET pulse) is connected to the AND Reset inputs of U321 and U322, through U320D, and to the $\overline{\text{Reset}}$ input of U326A. Since the other AND Reset inputs of U321 and U322 are connected to $\overline{\text{PRE}}$, which is low, no reset of U321 and U322 occurs. U326A, however, is reset. This brings the clock input of U328 low, incrementing the counter. U321 and U322 continue to count to 255, back to 0, and repeat the above sequence until U328 reaches the count of 6, which occurs after 1522 (5 x 256 + 242 = 1522) cycles of the 1200 Hz clock, or 1.268 seconds after the SEND switch is released.

When U328 reaches the count of 6, $\overline{PRE}$ goes high, and the above sequence is changed to the page sequence. The page sequence is similar to the above sequence, except that the $\overline{PRE}$ line is now high. Therefore the AND Reset inputs of U321 and U322 are not enabled, and U321 and U322 now are reset to 0 by the COUNT-RESET pulse. Therefore, the counter cycle is reduced to 242 cycles of the 1200 Hz clock. In addition, the clock input to U328 is disabled, since the output of U318 is low regardless of the state of the $\overline{COM}$ line.

Circuits U339D, U318B, U325A, B, and C form a gate whose output goes high while the count in U321 and U322 is 92 or 93, and $\overline{PRE}$ is high. This is the 1/2-bit signal described above. This 1/2-bit line is connected to one input of NOR gate U318C; the other input is connected to the $\overline{SEND}$ line. The output of this gate is low whenever either input is high; that is, when not sending, or during the 1/2-bit space. This output is MPX B. The 1/2-bit line is also connected to the J input of flip-flop U326B, which generates the $\overline{W2}$ Sync signal, as described above. The complement of $\overline{W2}$ Sync is combined with the 300 Hz output of U321, MPX A, and a signal which is high from the 88th count of U321 and U322 to the 94th count. This is present at a gate consisting of U338C, U324D, U327A, and U310B, and forms the SRCK 1 signal.

Signals $\overline{COM}$ and $\overline{PRE}$ are connected to NAND gate U327B to form MPX A, which is low when both $\overline{COM}$ and $\overline{PRE}$ are high; that is, it is low only during transmission of word 1, the 1/2-bit space, and word 2. U310A and U310C are connected as a 2-input NOR gate which combines the 1200 Hz output of U319 with the 600 Hz output of U321 to form SRCK 2. The COM signal is combined with the $\overline{PRE}$ signal in NAND gate U327C to give a signal which goes low when the comma is being sent. This signal is connected to the $\overline{Reset}$ input of Send flip-flop U317B through the SINGLE/CONT front panel switch. When this switch is in the SINGLE position, the line is connected, causing the Send flip-flop to be reset immediately after the conclusion of the transmission of word 2, thus sending a single-page sequence as shown in Figure 7.

j. Output Amplifier

This circuit, located on the power supply board (Figure 4) consists of U204, Q201 through 204, and CR207. U204 is used as a comparator. It compares either the normal or inverted output of the output multiplexer, as selected by the INVERT/NON-INVERT front panel switch, to a voltage of 1.4 volts, determined by voltage divider R212 and R213. If the input is less than this voltage, the output of U204 goes negative. If the output is greater than 1.4 volts, the output of U204 will be positive. The output of U204 is connected to a non-inverting power switch composed of Q201 through Q204. The output of this power switch will be +12 volts when U204

output is positive and -12 volts when it is negative. This output goes to a clipper consisting of R210, R211, and CR207, which limits the output to plus and minus voltages determined by the outputs of the symmetric bipolar power supply. The symmetry of these outputs is adjustable to assure equal positive and negative excursions of the clipped waveform.

k. Power Supply

The power supply (Figure 4) is in two sections. The first section supplies +5 volts, and consists of CR201, CR202, C201, C206, and U1 (on the main chassis; Figure 2), and the low-voltage winding of T1 (on the main chassis). The second section consists of two cascaded bipolar supplies, giving four separate voltage outputs. CR203 through 206, C202, C203, and the high-voltage winding of transformer T1 form a dual-voltage supply, whose outputs are regulated by fixed regulators U201 and U202 to give +12 volts and -12 volts, respectively. These outputs, besides being available for use directly, are used to supply power to the dual voltage tracking regulator consisting of U203 and associated components. C207 and C208 are compensation capacitors to stabilize the regulator against high-frequency oscillations. R201 and R202 are current sensing resistors for short-circuit protection. R203 is the feedback resistor which sets the positive output voltage to the value of the internal reference (about 8 volts). R206, 207, and 208 form an adjustable voltage divider which adjusts the symmetry of the dc output by adjusting the negative output voltage. R205 and R209 are static load resistors which give the circuit the capability of sinking, as well as sourcing, current. C209 and C210 are output capacitors which improve the transient response of the circuit.

6. PARTS LISTS

SP49008411 Main Chassis

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		CAPACITOR, Fixed
C1, 2, 3	21-847070	800 pF CER. DISC.
		SEMICONDUCTOR DEVICE, Diode:
DS1, 2, 3	4805174A02	LED
		FUSE:
F1	6500138592	1/2 Amp. Slow Blow type
		JACK:
J1		Consists of: 1483734D01 Insulator, 4600865778 Red Binding post, 4600865779 Black Binding post
J2	0983840H04	Connector
		RESISTOR:
R1	1807168C01	pot.; 500 Ω ±10%
R2, 3, 4	0600006373	150 Ω ±10%; 1/2 W
R5	0600128689	2.2 k ±10%; 1/4 W
		SWITCH:
S1	4082268G02	Rotary; 2P3T
S2	4007175C01	Toggle; SPDT
S3	4082372A01	Pushbutton; SPDT
		TRANSFORMER:
T1	2507147C01	Power
		INTEGRATED CIRCUIT:
U1	5107166C01	Voltage regulator; type LM323K
		CORD:
W1	3082494J05	Line; and plug
	NONREFERENCED ITEMS	
	0200001362	NUT, 6-32; 15 req'd
	0200115013	NUT, 3/8-32; 4 req'd
	0200120487	NUT, 2-56; 4 req'd
	0200120908	NUT, 15/32-32
	0300001977	SCREW, 6-32 x 3/8; 15 req'd
	0300001983	SCREW, 6-32 x 1/2; 8 req'd
	0300400100	SCREW, 4-40 x 3/8; 2 req'd

SP49008411 Main Chassis (cont'd)

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
	NONREFERENCED ITEMS	
	0300490773	SCREW, 6-32 x 9/16; 4 req'd
	0400002645	LOCKWASHER, #6; 22 req'd
	0400008424	LOCKWASHER, 15/32
	0400114582	LOCKWASHER, #4; 2 req'd
	0400114970	WASHER, Flat; #4, 2 req'd
	0400127598	WASHER, Flat; #6, 28 req'd
	0707131C01	BRACKET
	0707132C01	BRACKET
	0982673A01	SOCKET
	1307148C01	ESCUTCHEON
	1507136C01	COVER, Housing
	1607173C01	TILT-STAND and FEET
	2707135C01	HOUSING
	2900005379	LUG, Double
	2982525J01	TERMINAL, 14 req'd
	3100120365	STRIP, Terminal; 3-contact
	3100121479	STRIP, Terminal; 6-contact
	3100832961	STRIP, Barrier; 3-terminal
	3607183C01	KNOB
	4282018H10	STRAIN RELIEF

SP49008412 Power Supply

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		CAPACITOR, Fixed:
C201	2307156B02	9000 uF; 15 V
C202, 203	2307156B01	2000 uF; 50 V
C204, 205, 206	2382256J07	4.7 uF; 63 V
C207, 208	2182187B11	.0015 uF ±10%
C209, 210	2383441B09	100 uF; 10 V
		SEMICONDUCTOR DEVICE, Diode:
CR201, 202	4807152B01	silicon
CR203 thru 206	4882466H13	silicon
CR207	4807176C01	silicon

SP49008412 Power Supply (cont'd)

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		TRANSISTOR:
Q201	4800869721	NPN; type M9721
Q202	4800869722	PNP; type M9722
Q203	4800869760	PNP; type M9760
Q204	4800869759	NPN; type M9759
		RESISTOR, Fixed: Ω
R201, 202	0600129755	10 ±10%; 1/4 W
R203	0600127802	1 k ±10%; 1/4 W
R205	0600006398	220 ±10%; 1 W
R206	0600129668	10 k ±5%; 1/4 W
R207	1807167C01	pot.
R208	0600129668	10 k ±5%; 1/4 W
R209	0600006389	220 ±10%; 1 W
R210	0600006373	150 ±10%; 1/2 W
R211	0600006326	100 ±10%; 1/2 W
R212	0600129819	3.9 k ±5%; 1/4 W
R213, 214	0600129668	10 k ±5%; 1/4 W
R215, 216	0600008689	2.2 k ±10%; 1/4 W
R217, 218	0600129668	10 k ±5%; 1/4 W
		INTEGRATED CIRCUIT:
U201	5184320A59	type MC7912CP
C202	5107166C03	type MC7812CP
U203	5107166C02	type MC1468L
U204	5184320A56	type MC1741SCP1
NONREFERENCED ITEMS		
	0300001413	SCREW, 4-40 x 5/16; 2 req'd
	0300115213	SCREW, 3-48 x 1/4; 2 req'd
	0400844093	WASHER
	2607178C01	HEATSINK

SP49008413 Main Logic Board

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		CAPACITOR, Fixed:
C301	2382256J05	100 uF; 10 V
C302	2382256J01	47 uF; 25 V
C303	2184511B91	10 pF ±.5 pF; N150
C304	2182428B21	.01 uF +80-20%
C305	2184511B91	10 pF ±.5 pF; N150
C306 thru 312	2183596E13	.001 uF ±10%
		TRANSISTOR:
Q301 thru 304	4800869721	NPN; type M9721
Q305	4800869648	NPN; type M9648
		RESISTOR, Fixed: Ω ±10%; 1/4 W
R301 thru 314	0600129683	390
R315 thru 322	0600129225	10 k
R323 thru 327	0600128689	2.2 k
R328, 329	0600127802	1 k
R330	0600128689	2.2 k
R331, 332	0600129225	10 k
R333	0600127802	1 k
R334	0600129228	330 k
R335	0600128902	47 k
R336	0600129228	330 k
R337, 338	0600128685	22 k
R339 thru 341	0600128689	2.2 k
R342 thru 353	0600128687	6.8 k
R354, 355	0600128689	2.2 k
		INTEGRATED CIRCUIT:
U301 thru 309	5184084D49	type SN74184N
U310	5184084D29	type SN7405N
U311	5184720F01	ROM
U312, 313	5184084D29	type SN7405N
U314, 315, 316	5184084D31	type SN7486N
U317	5184084D13	type SN7473N
U318	5184792E02	type SN74L02N
U319	5184084D18	type SN7493AN
U320	5184084D01	type SN7400N
U321, 322	5184084D18	type SN7493AN
U323	5184084D30	type SN7411N
U324	5184084D03	type SN7402N
U325	5184084D30	type SN7411N
U326	5184084D13	type SN7473N

SP49009413 Main Logic Board (cont'd)

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
U327	5184084D41	type SN7437N
U328	5184084D62	type SN7492AN
U329	5184084D13	type SN7473N
U330, 331, 332	5184084D66	type SN74157N
U333, 334, 335	5184805E38	type SN7495AJ
U336	5184688D31	type MC4008P
U337	5184084D65	type SN74153N
U338	5184084D31	type SN7486N
U339	5184084D29	type SN7405N
		CRYSTAL:
Y301	4807164C01	19.2 kHz
NONREFERENCED ITEM		
	1400861196	INSULATOR (for Y301)

SP49008414 Leverwheel Interface Board

REFERENCE SYMBOL	MOTOROLA PART NO.	DESCRIPTION
		JACK:
J401	0983840H03	Connector, 44-pin
		ASSY, Leverwheel:
S401	4007146C01	6-station with 2 blanks
NONREFERENCED ITEM		
	2982524J01	PIN, Terminal, 14 req'd

7. ATTACHMENTS

Figure 1	Binary Digital Test Encoder, Block Diagram	2-SP490084
Figure 2	Binary Digital Test Encoder, Main Chassis, Schematic Diagram	3-SP490084
Figure 3	Binary Digital Test Encoder, Leverwheel Board, Schematic Diagram	6-SP490084
Figure 4	Binary Digital Test Encoder, Power Supply Board, Schematic Diagram	4-SP490084
Figure 5	Binary Digital Test Encoder, Main Logic Diagram	7-SP490084
Figure 6	Binary Digital Test Encoder, Timing Diagram, Continuous Mode	8-SP490084
Figure 7	Binary Digital Test Encoder, Timing Diagram, Single-Page Mode	9-SP490084
Figure 8	Binary Digital Test Encoder, Component Layout Diagram, Logic Board	11-SP490084
Figure 9	Binary Digital Test Encoder, Component Layout Diagram, Power Supply Board	12-SP490084

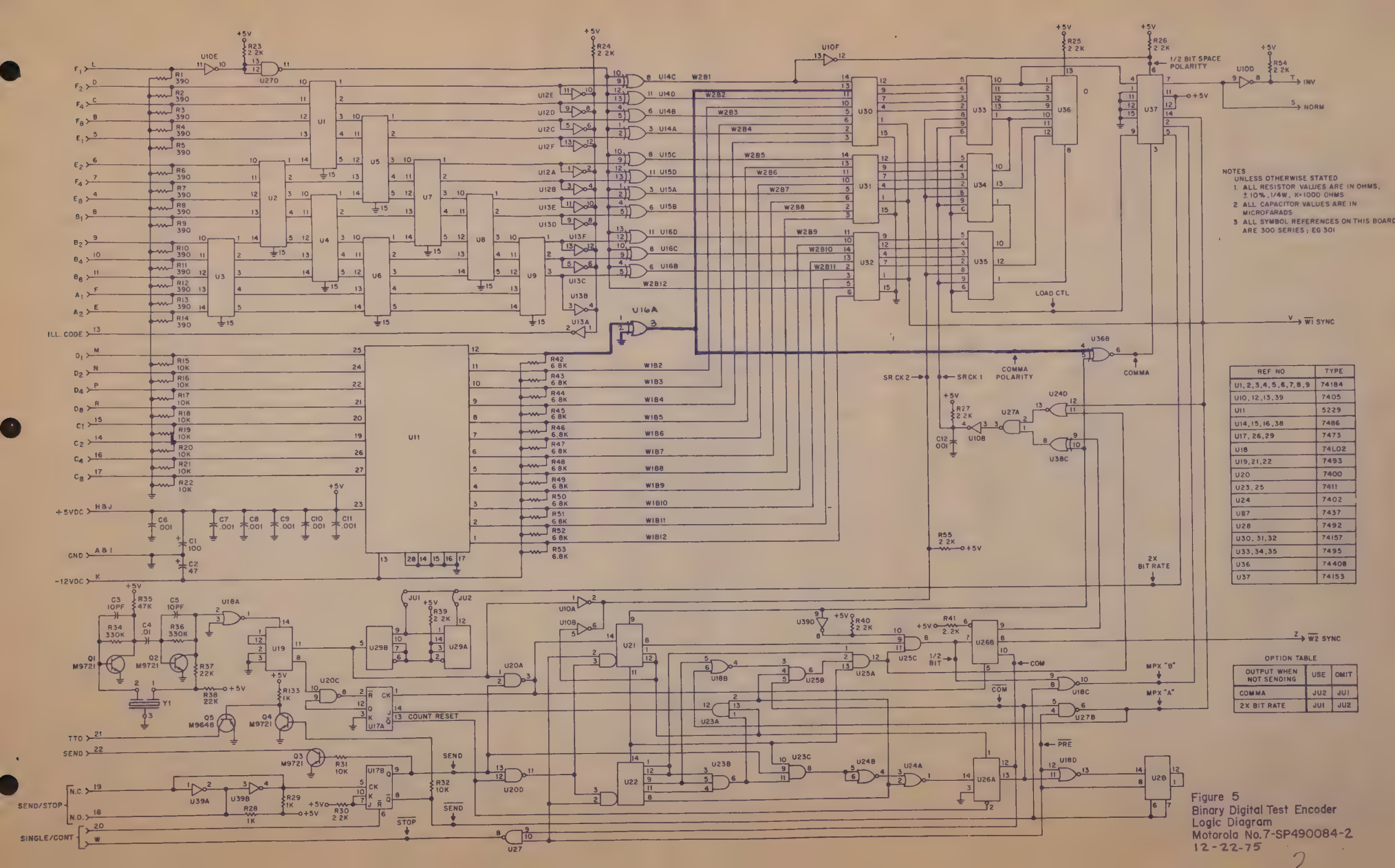


Figure 5
Binary Digital Test Encoder
Logic Diagram
Motorola No.7-SP490084-2
12-22-75

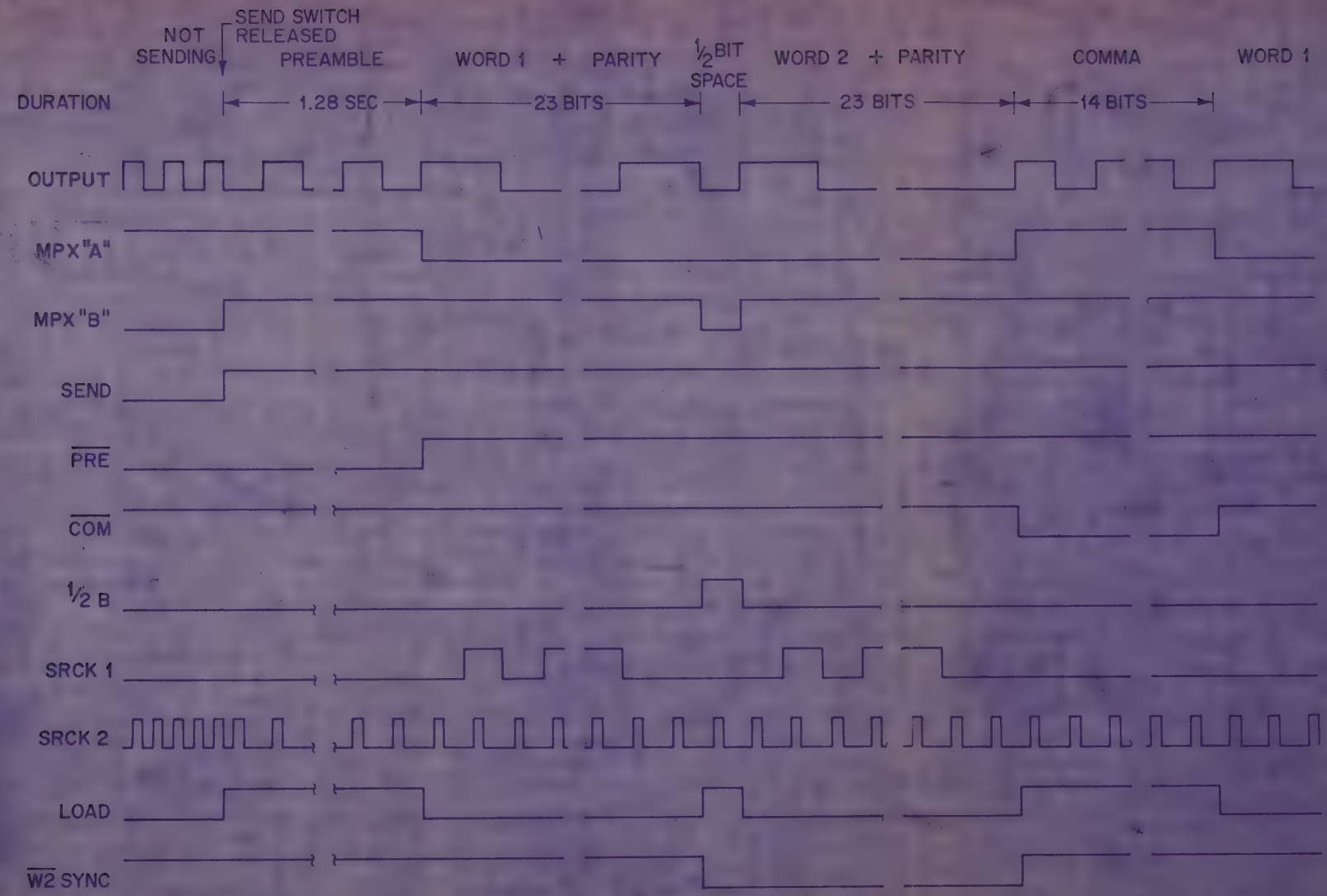


FIGURE 6
BINARY DIGITAL ENCODER
TIMING DIAGRAM-CONTINUOUS MODE
MOTOROLA NO. 8-SP490084-1

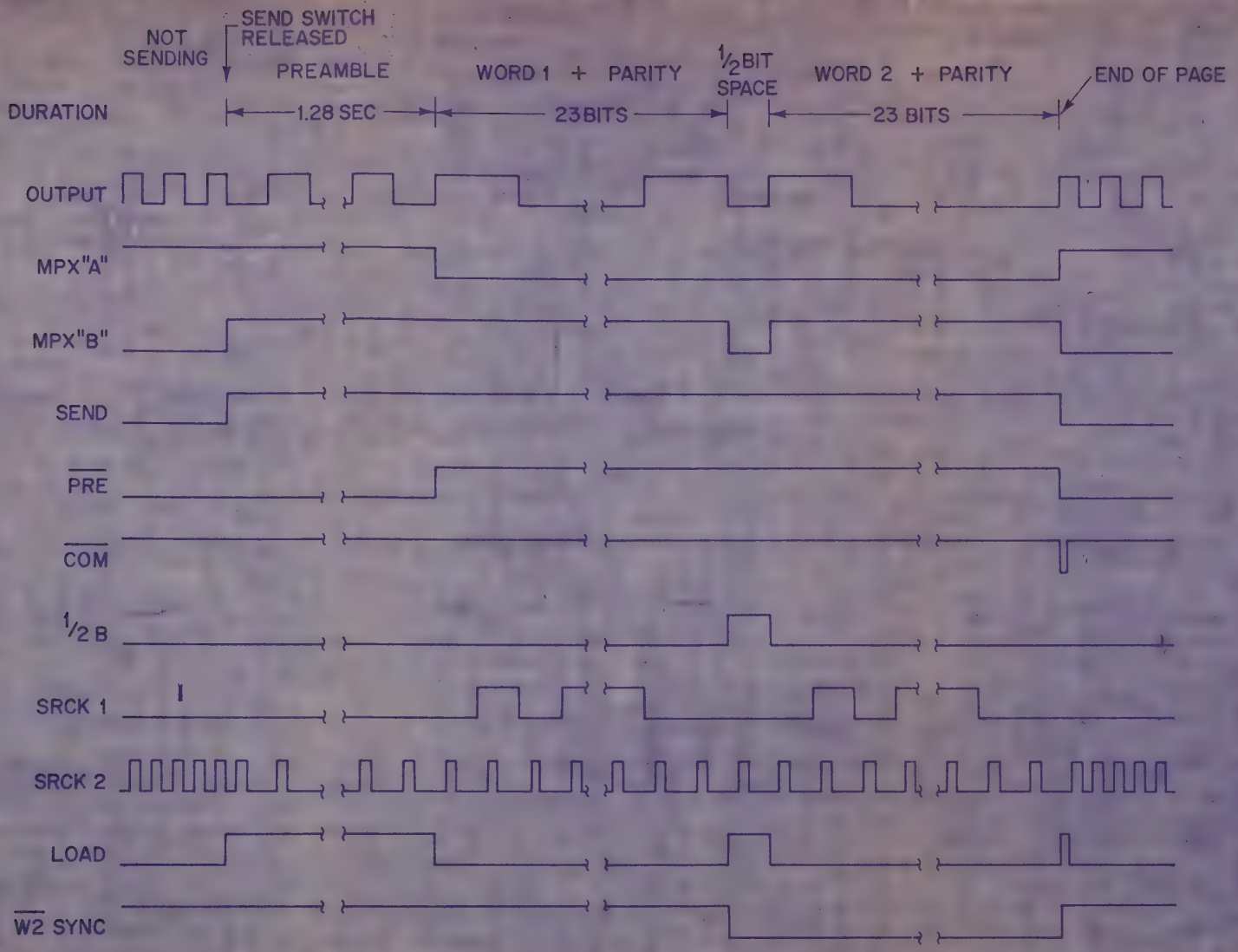


FIGURE 7
BINARY DIGITAL ENCODER
TIMING DIAGRAM–SINGLE PAGE MODE
MOTOROLA NO. 9-SP490084-1

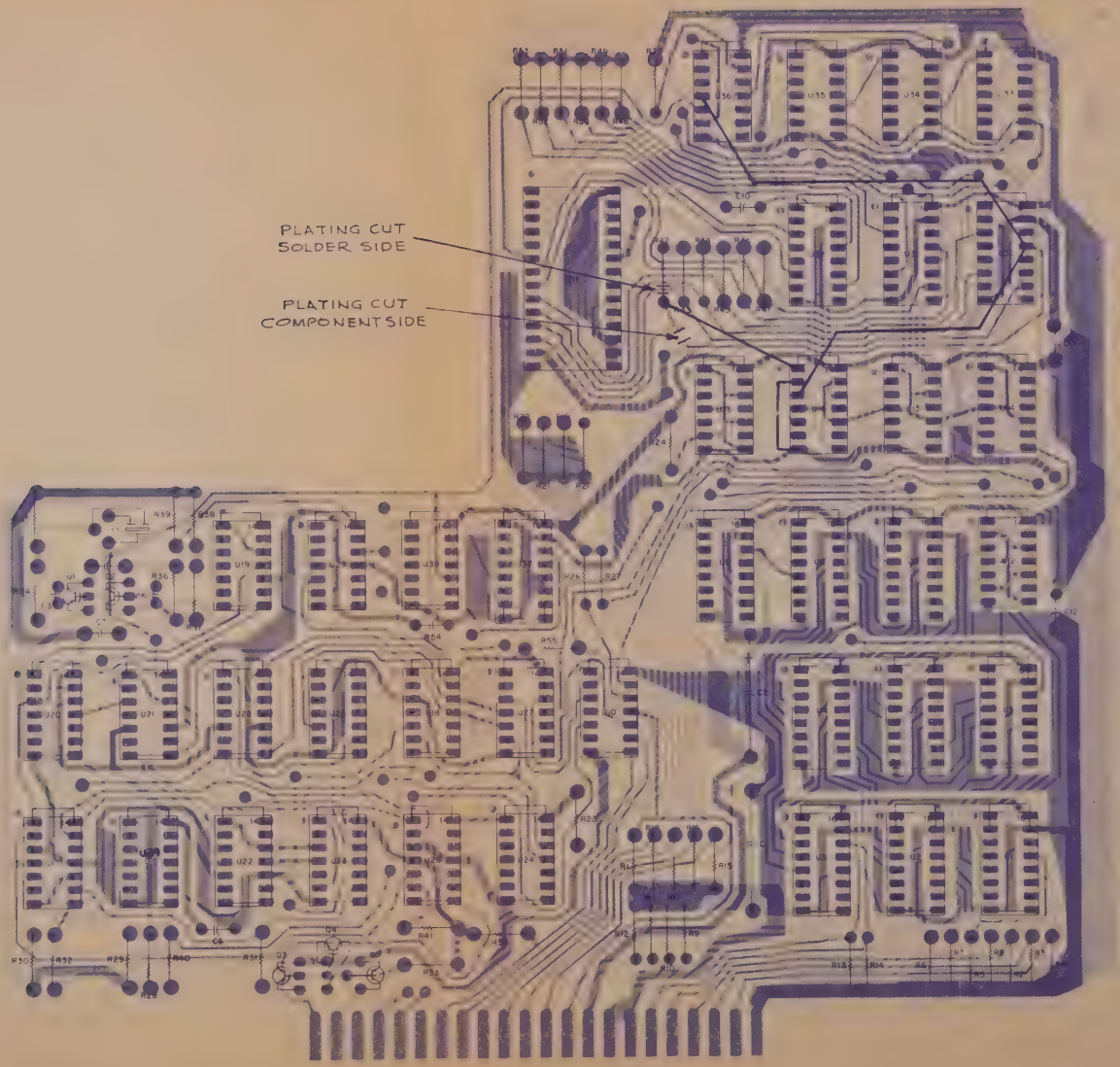


Figure 8
Logic Board
Binary Digital Test Encoder
Component Layout Diagram
Motorola No. 11-SP490084-2
12-22-75

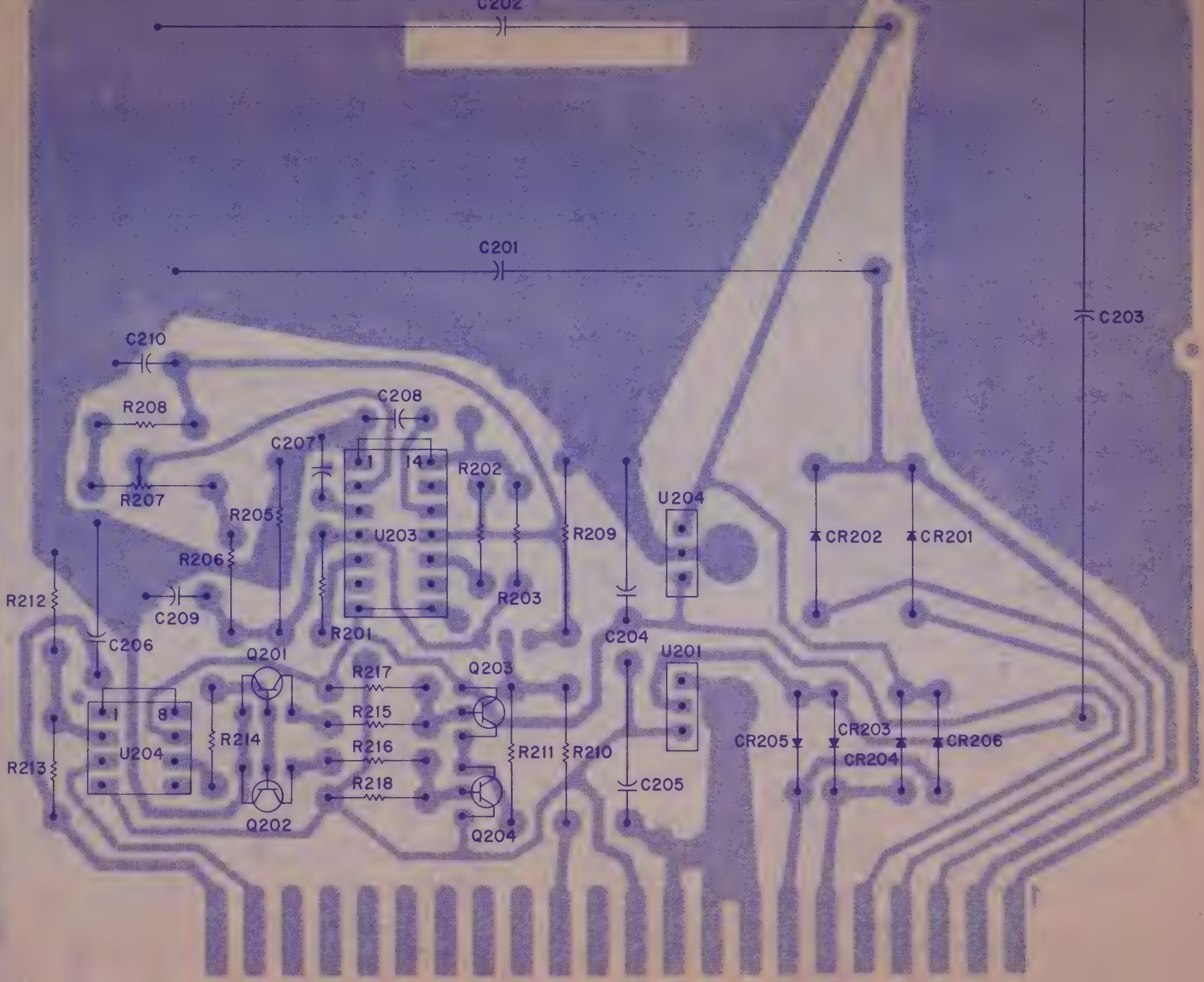


Figure 9
Power Supply Board
Binary Digital Test Encoder
Component Layout Diagram
Motorola No. 12-SP490084-1
8/28/74

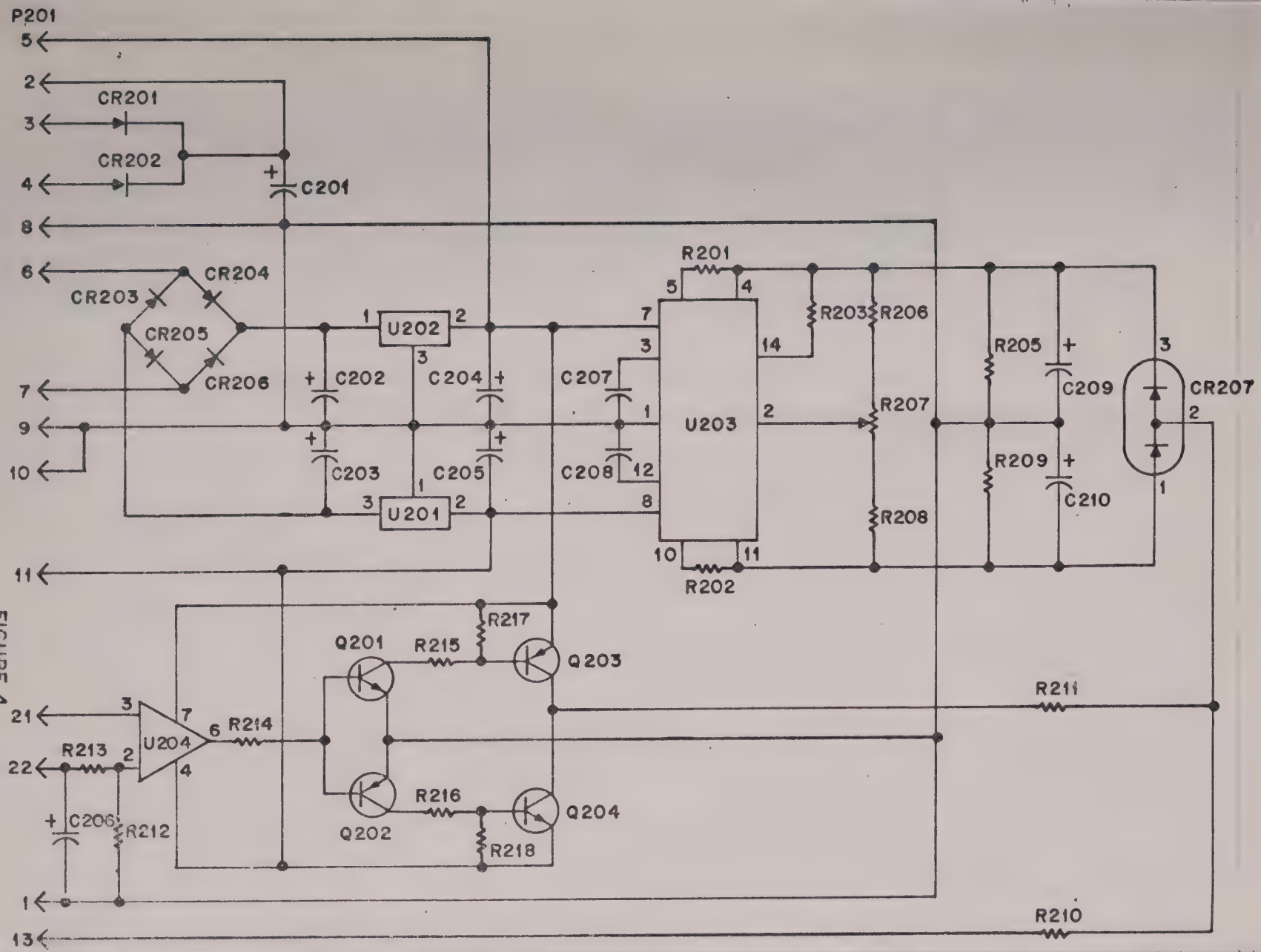
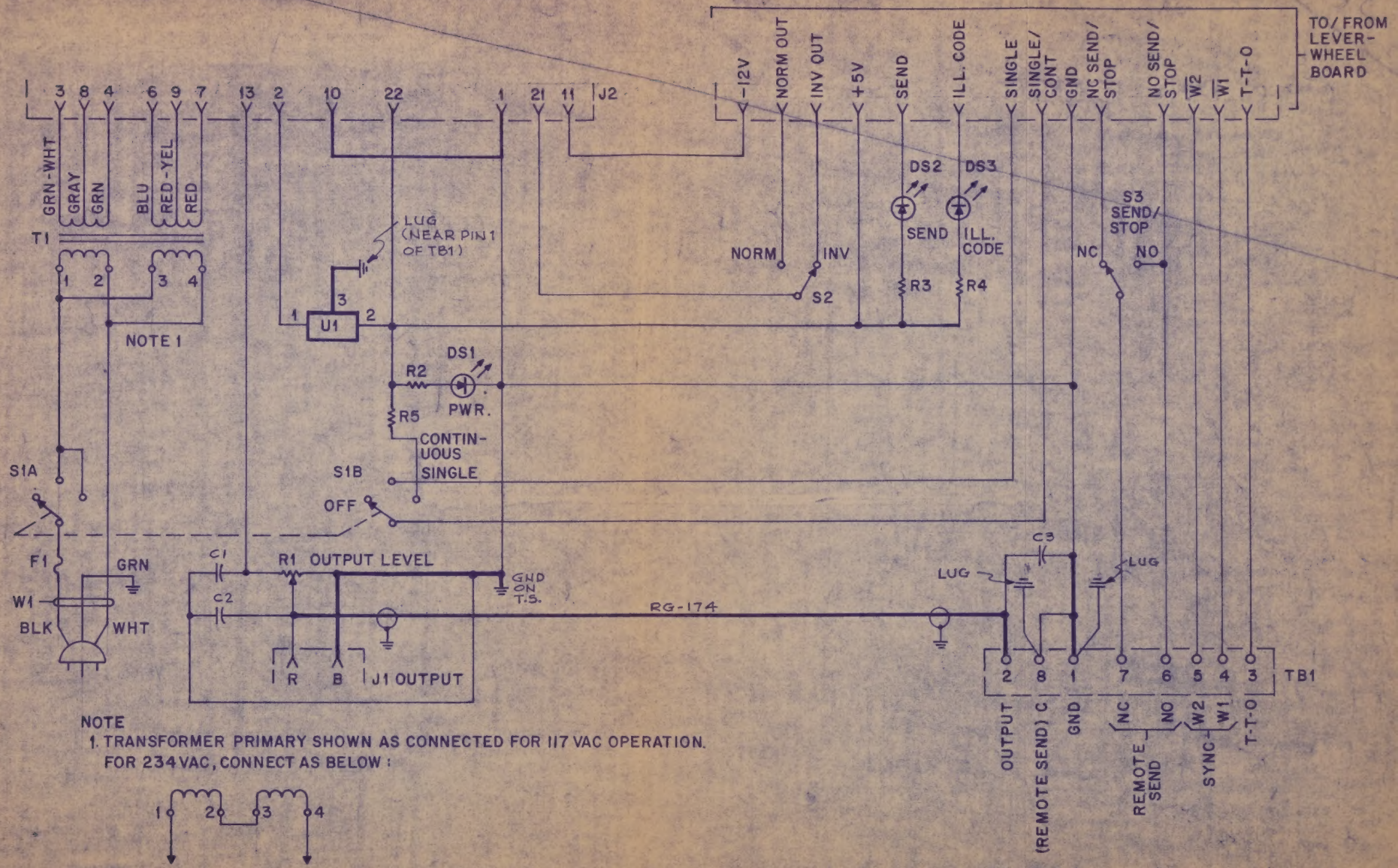


FIGURE 4
BINARY DIGITAL TEST ENCODER
POWER SUPPLY BOARD
SCHEMATIC DIAGRAM
MOTOROLA NO. 4-SP49008A4-1
6-12-74

F



NOTE

1. TRANSFORMER PRIMARY SHOWN AS CONNECTED FOR 117 VAC OPERATION. FOR 234 VAC, CONNECT AS BELOW :

FIGURE 2
BINARY DIGITAL TEST ENCODER, MAIN CHASSIS
SCHEMATIC DIAGRAM
MOTOROLA NO. 3-SP490084-2
12-22-75